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REMARKS/ARGUMENTS

Claims 1 and 4 are pending in this application. By this Amendment, Applicant AMENDS the Drawings and claims 1 and 4 and CANCELS claims 2, 3, 5, and 6.

Applicant has canceled claims 2, 3, 5 and 6 as being directed to non-elected species. Applicant reserves the right to file a Divisional Application to pursue examination and allowance of claims 2, 3, 5 and 6.

The Drawings were objected to for failing to designate Fig. 3 as --Prior Art--. Applicant has amended Fig. 3 to properly be designated as --Prior Art--. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the objection to the Drawings.

Claims 1 and 4 were rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Miyauchi (US 5,717,886). Applicant respectfully traverses the rejection of claims 1 and 4.

Claim 1 has been amended to recite:

"A data processing device comprising:
a read-only memory;
a flash memory capable of modifying information stored therein and adding information thereto;
a central processing unit performing data processing using information stored in said read-only memory and said flash memory;
an information storage area provided in said flash memory for storing predetermined modifiable information among the information used by said central processing unit for data processing;
an address storage area provided in said flash memory for storing at least the address of the information stored in said information storage area; and
an address-modification control unit for, after at least one of modification of modifiable information stored in said information storage area and addition of modifiable information to said information storage area, and in accordance with said one of the modification of the information and addition of the information, performing one of modification of the address of the information stored in said address storage area and addition of the address of the information to said address storage area; wherein

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the information used by said central processing unit for data processing can be freely modified or added; and
the address-modification control unit controls a function address table area and a variable address table area." (emphasis added)

Claim 4 has been amended to recite:

"A method in a data processing device comprising:
a read-only memory;
a flash memory capable of modifying information stored therein and adding information thereto;
a central processing unit performing data processing using information stored in said read-only memory and said flash memory;
an information storage area in said flash memory; and
an address storage area in said flash memory;
said method comprising the steps of:
storing in said information storage area predetermined modifiable information among the information used by said central processing unit for data processing;
storing in said address storage area at least the address of the information stored in said information storage area;
performing at least one of modification of modifiable information stored in said information storage area and addition of modifiable information to said information storage area; and
then, in accordance with said one of modification of the information and addition of the information, performing one of modification of the address of the information, stored in said address storage area and addition of the address of the information to said address storage area;
wherein
the information used by said central processing unit for data processing can be freely modified or added; and
the address storage area includes a function address table area and a variable address table area." (emphasis added)

Applicant's claim 1 recites the feature of "the address-modification control unit controls a function address table area and a variable address table area." Applicant's claim 4 recites the feature of "the address storage area includes a function address table area and a variable address table area." With the improved features of claims 1 and 4, Applicant has been able to provide a data processing device in which the main

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program and information regarding functions can be freely modified (see, for example, the fourth full paragraph on page 2 of the originally filed Specification).

Applicant agrees with the Examiner that AAPA fails to teach or suggest the features of an address modification control unit or an address storage area. The Examiner has relied upon Miyauchi to allegedly cure this deficiency.

Applicant has amended claim 1 to recite the feature of "the address-modification control unit controls a function address table area and a variable address table area." Applicant has amended claim 4 to recite the feature of "the address storage area includes a function address table area and a variable address table area."

Because AAPA fails to teach or suggest the features of an address modification control unit or an address storage area, AAPA clearly fails to teach or suggest the feature of "the address-modification control unit controls a function address table area and a variable address table area" as recited in Applicant's claim 1 or the feature of "the address storage area includes a function address table area and a variable address table area" as recited in Applicant's claim 4.

Further, as described in lines 38-65 of column 3, Miyauchi is directed to determining a conversion table between Logic Sector Addresses and Physical Sector Address for any information that is stored in the flash memory 104. Miyauchi clearly fails to differentiate the information to be stored in the flash memory 104 into functions and variables as recited in Applicant's claimed invention. Thus, Miyauchi clearly fails to teach or suggest the feature of "the address-modification control unit controls a function address table area and a variable address table area" as recited in Applicant's claim 1 or the feature of "the address storage area includes a function address table area and a variable address table area" as recited in Applicant's claim 4.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1 and 4 under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Miyauchi.

Accordingly, Applicant respectfully submits that AAPA and Miyauchi, applied

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alone or in combination, fail to teach or suggest the unique combination and arrangement of elements and method steps recited in claims 1 and 4 of the present application.

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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